

*Sub C<sup>2</sup>*

21. A semiconductor device comprising:  
2       an exterior surface having a top level of metallurgy,  
3       wherein an exposed portion of said top level of metallurgy comprises a bonding pad, and  
4       wherein an upper 10% to 20% of said bonding pad comprises a silicided surface.

*Sub C<sup>1</sup>*

22. The semiconductor device in claim 21, wherein a bottom 80% to 90% of said bonding pad is free of silicide.

*Sub C<sup>1</sup> B<sup>1</sup> Cont*

23. The semiconductor device in claim 22, wherein said silicided surface is free of oxides and silicide islands.

1       24. The semiconductor device in claim 23, wherein, prior to formation of said silicided  
2       surface, said bonding pad is cleaned by applying one of an ammonia plasma and a hydrogen  
3       plasma to make said bonding pad free of said oxides and silicide islands.

1       25. The semiconductor device in claim 21, further comprising a terminal connected to said  
2       bonding pad, wherein a thickness of said silicided surface increases adhesion between said  
3       terminal and said bonding pad.

1       26. The semiconductor device in claim 25, wherein said terminal comprises one of a lead and  
2       tin solder.

1       27. The semiconductor device in claim 21, further comprising at least one internal level of  
2       metallurgy within an interior of said semiconductor device, wherein said top level of metallurgy  
3       is thicker than said internal level of metallurgy.

1       28. The semiconductor device in claim 21, wherein said top level of metallurgy comprises  
2       copper.

Subt C<sup>3</sup>

1        29. A semiconductor chip comprising:  
2              an exterior surface having a top level of metallurgy; and  
3              an interior having at least one internal level of metallurgy,  
4              wherein said top level of metallurgy is thicker than said internal level of metallurgy,  
5              wherein an exposed portion of said top level of metallurgy comprises a bonding pad, and  
6              wherein an upper 10% to 20% of said bonding pad comprises a silicided surface.

Subt C<sup>3</sup>  
1        30. The semiconductor device in claim 29, wherein a bottom 80% to 90% of said bonding  
2              pad is free of silicide.

1        31. The semiconductor device in claim 30, wherein said bonding pad is free of oxides and  
2              silicide islands.

1        32. The semiconductor device in claim 31, wherein, prior to formation of said silicided  
2              surface, said bonding pad is cleaned by applying one of an ammonia plasma and a hydrogen  
3              plasma to make said bonding pad free of said oxides and silicide islands.

1        33. The semiconductor device in claim 29, further comprising a terminal connected to said  
2              bonding pad, wherein a thickness of said silicided surface increases adhesion between said  
3              terminal and said bonding pad.

1        34. The semiconductor device in claim 33, wherein said terminal comprises one of a lead and  
2              tin solder.